CLAIMS

What is claimed is:

1. A random access memory comprising:

a controlled high voltage supply;

word lines;

memory cells, each comprising a charge storage capacitor and a pass transistor for storing a logic level on the storage capacitor, the pass transistor having an enable input connected to a word line;

word line selection circuits, each selection circuit comprising:

a pair of cross-coupled transistors coupled drain-to-gate at respective control nodes and having respective sources coupled to the controlled high voltage supply;

a first pull-down transistor coupled to one of the control nodes and gated by a word line select signal; and

a second pull-down transistor connected in parallel with the first pull-down transistor to said one of the control nodes, the gate of the second pull-down transistor being coupled to the other control node.